CLAIMS

1. A method of decoding serially received data bits encoded on a bus voltage as a pattern of first and second logic levels, the method comprising the steps of:

identifying a start and an end of each data bit;

initializing a counter value to a starting value when the start of a data bit is identified;

detecting the logic level of the bus voltage;

incrementing the counter value at a predefined rate so long as the detected logic level is the first logic level;

decrementing the counter value at a predefined rate so long as the detected logic level is the second logic level; and

when the end of the data bit is identified, comparing the counter value to the starting value to decode the logic level of the data bit.

2. The method of Claim 1, wherein the data bits are encoded as a first logic level period followed by a second logic level period, with the first logic level period exceeding the second logic level period for a data bit of the first logic level, and the second logic level period exceeding the first logic level period for a data bit of the second logic level, including the steps of:

decoding the logic level of the data bit as the first logic level when the counter value is above the starting value; and

decoding the logic level of the data bit as the second logic level when the counter value is below the starting value.

3. The method of Claim 1, wherein the step of identifying the start and end of each data bit includes the step of:

low-pass filtering the bus voltage; and

comparing the filtered bus voltage to a voltage threshold intermediate first and second reference voltages corresponding to the first and second logic levels.

4. Apparatus for decoding serially received data bits encoded on a bus voltage as a pattern of first and second logic levels, comprising:

an oscillator producing clock pulses at a fixed clock frequency;

a bi-directional counter for counting the clock pulses of said oscillator;

initialization means for initializing said bi-directional counter to a starting value at a start of each data bit;

direction control means for configuring the counter to count the clock pulses in a first direction so long as the bus voltage is at said first logic level, and to count the clock pulses in a second direction so long as the bus voltage is at said second logic level; and

a bit decoder for sampling a count of said counter at an end of the data bit and decoding the logic level of the data bit by comparing the sampled count to the starting value.

5. The apparatus of Claim 4, wherein the data bits are encoded at a transmission frequency that is at least as great as a minimum transmission frequency, the starting value is substantially one-half of a maximum count of the counter, and said maximum count is sufficiently large to prevent an overflow of said counter when the data bits are encoded at said minimum transmission frequency.

6. The apparatus of Claim 4, wherein the data bits are encoded as a first logic level period followed by a second logic level period, with the first logic level period exceeding the second logic level period for a data bit of the first

logic level, and the second logic level period exceeding the first logic level period for a data bit of the second logic level, and wherein:

said bit decoder decodes the logic level of the data bit as the first logic level when the sampled count exceeds the starting value; and

said bit decoder decodes the logic level of the data bit as the second logic level when the starting value exceeds the sampled count.

7. The apparatus of Claim 4, wherein said direction control means comprises:

a low-pass filter for filtering noise out of the bus voltage; and

a comparator for comparing the filtered bus voltage to a voltage threshold intermediate first and second reference voltages corresponding to the first and second logic levels.